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EXAMINER
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CUTLER, ALBERT H

ART UNIT	PAPER NUMBER
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2622

NOTIFICATION DATE	DELIVERY MODE
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ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/811,840	<b>Applicant(s)</b> SASAKI, GEN	
	<b>Examiner</b> ALBERT H. CUTLER	<b>Art Unit</b> 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 29 June 2010.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-9, 13-16 and 20-27 is/are pending in the application.
- 4a) Of the above claim(s) 3-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 13-16 and 20-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)                        | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is responsive to communication filed on June 29, 2010. Claims 1-9, 13-16 and 20-27 are pending in the application. Claims 3-9 are withdrawn from consideration. Claims 1, 2, 13-16 and 20-27 have been examined by the Examiner.

#### ***Continued Examination Under 37 CFR 1.114***

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 1, 2010 has been entered.

#### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1, 2, 13-16 and 20-27 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Claim Objections***

4. Claim 1 is objected to because of the following informalities: Lack of clarity and precision.

Claim 1 recites at line 12, "an output said buffer memory". Claim 1 should be amended to recite "an output **of** said buffer memory", or something of similar nature, in order to improve clarity and conform to proper idiomatic English. Appropriate correction is required.

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5. Claim 24 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 24 recites "said compression unit compressing said image data read from said buffer memory and storing compressed image data in said storage unit". Parent claim 1 previously recites "a compression unit for compressing said image data read from said buffer memory and outputting compressed image data to said storage unit". Claim 24, as currently written, does not further limit claim 1.

The objections previously made to claims 18 and 19 are hereby removed in view of Applicant's response.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 and 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Anderson (US 6,563,535).

Consider claim 1, Anderson teaches:

An image processing apparatus (digital camera, figure 1) for performing image processing on captured data of an image of a desired subject (The camera contains a digital signal processor (106) which performs image processing, column 4, lines 24-30, figures 1 and 2B.), comprising:

- an image processing part (DSP, 106, figures 1 and 2B); and

- a storage unit (memory, 109) provided outside said image processing part (106) and connected to said image processing part (106) by a bus (The storage unit (109) is connected to said image processing part (106) by a bus (113), figure 2B, column 5, lines 56-61.),

- said image processing part (106) including:

- a buffer memory (MCU buffer, 204) for data storage (The MCU buffer (204) is used to store displayable image data prior to inputting it to JPEG block (205), column 5, lines 17-19.);

- an image processing unit (image processing data path, 202) for performing a predetermined process on said captured data to obtain image data ("takes the raw CCD data and converts it into a real image data capable of being displayed", column 5, lines 4-16), and writing said image data to said buffer memory (See figure 2B. The image processing unit (202) outputs the image data to the buffer memory (204).); and

- a compression unit (JPEG block, 205) for compressing said image data read from said buffer memory (204) and outputting compressed image data to said storage unit ("A buffer 204 is used to coordinate the transfer of displayable image data to the

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JPEG block 205, which compresses the data. The compressed displayable image data is then stored in file buffer 213.” column 5, lines 17-20, see figure 2B),

wherein an input of said buffer memory (204) is connected, separate from said bus (113), only to said image processing unit (202) to receive only said image data from said image processing unit (See figure 2B. The upper-left input of the buffer memory (204) is connected, separate from said bus (113), only to said image processing unit (202).), and

an output said buffer memory (204) is connected, separate from said bus (113), only to said compression unit (205) to output said image data only to said compression unit (See figure 2B. The lower-right output of the buffer memory (204) is connected, separate from the bus (113), only to said compression unit (205).),

wherein said compression unit (205) is connected to said bus (113, see figure 2B) and outputs said compressed image data directly to said storage unit via said bus (“A buffer 204 is used to coordinate the transfer of displayable image data to the JPEG block 205, which compresses the data. The compressed displayable image data is then stored in file buffer 213.” column 5, lines 17-20, see figure 2B. The bus (113) connects the image processing part (106) to the storage unit (109), figure 2B, column 5, lines 56-61.).

Consider claim 22, and as applied to claim 1 above, Anderson further teaches:  
said image processing part (106) comprises:

a first processing unit (capture data path, 201) for performing a first processing on said captured data and for storing first processed data in said storage unit ("Some of its function include controlling the CCD driver, performing slight compression, collecting statistics regarding the raw CCD data, generating timing references, and loading the input buffer 210 with the slightly compressed raw data." column 4, line 63 through column 5, line 2, figure 2B.); and

a second processing unit (image processing data path, 202) for performing a second processing on said first processed data obtained from said storage unit and outputting said image data to said buffer memory ("takes the raw CCD data and converts it into a real image data capable of being displayed", column 5, lines 4-16. See figure 2B. The image processing unit (202) outputs the image data to the buffer memory (204).).

Consider claim 23, and as applied to claim 1 above, Anderson further teaches:  
said image processing part (106) connected to store data in and retrieve data from said storage unit (The image processing part (106) is connected to the storage unit (109) via the bus (113), column 5, lines 56-61.).

Consider claim 24, and as applied to claim 1 above, Anderson further teaches:  
said compression unit (205) compressing said image data read from said buffer memory (204) and storing compressed image data in said storage unit ("A buffer 204 is used to coordinate the transfer of displayable image data to the JPEG block 205, which

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compresses the data. The compressed displayable image data is then stored in file buffer 213." column 5, lines 17-20, see figure 2B).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 2, 13-16, 20, 21, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 6,563,535) in view of Kuo et al. (US 6,400,471).

Consider claim 2, and as applied to claim 1 above, Anderson further teaches that double buffering is performed (column 13, lines 54-57), and that the MCU buffer (204) holds two MCU's (column 14, lines 10-14). Anderson also teaches that alternate embodiments of the MCU input buffers are contemplated to be within the scope of the present invention (column 14, lines 4-7).

However, Anderson does not explicitly teach that said buffer memory includes a first buffer memory and a second buffer memory, said image processing apparatus further comprising a control unit being operative in such a manner that while said image processing unit writes said image data either to said first buffer memory or to said second buffer memory, said compression unit selectively reads image data previously stored either in said first buffer memory or in said second buffer memory experiencing no writing of said image data by said image processing unit.

Kuo et al. similarly teaches an image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising an image processing unit (DSP, 922, figure 11) connected to a buffer memory (Ping-Pong Buffers A and B, 1130), which is in turn connected to a compression unit (JPEG hardware, 924).

However, in addition to the teachings of Anderson, Kuo et al. teaches that the buffer memory (ping-pong buffers A and B, 1130) includes a first buffer memory (A) and a second buffer memory (B), said image processing apparatus further comprising:

a control unit (CPU, 344, figure 2) being operative (column 5, lines 42-54) in such a manner that while said image processing unit (922) writes said image data either to said first buffer memory (A) or to said second buffer memory (B), said compression unit (924) selectively reads image data previously stored either in said first buffer memory (A) or in said second buffer memory (B) experiencing no writing of said image data by said image processing unit (See column 11, lines 36-46. One buffer is filled with image data from the DSP (922) while the other buffer is output to the JPEG hardware (924).).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the buffer memory taught by Anderson comprise ping-pong buffers as taught by Kuo et al. as a way of applying a known technique (i.e. ping-pong buffering as taught by Kuo et al.) to a known device (i.e. the image processing apparatus of Anderson) ready for improvement to yield predictable results such as increased processing efficiency due to the parallel processing ping-pong buffering technique.

Consider claim 13, and as applied to claim 1 above, Anderson further teaches that double buffering is performed (column 13, lines 54-57), and that the MCU buffer (204) holds two MCU's (column 14, lines 10-14). Anderson also teaches that alternate embodiments of the MCU input buffers are contemplated to be within the scope of the present invention (column 14, lines 4-7).

However, Anderson does not explicitly teach a first switching unit connected between said image processing unit and said buffer memory, and a second switching unit connected between said compression unit and said buffer memory.

Kuo et al. similarly teaches an image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising an image processing unit (DSP, 922, figure 11) connected to a buffer memory (Ping-Pong Buffers A and B, 1130), which is in turn connected to a compression unit (JPEG hardware, 924).

However, in addition to the teachings of Anderson, Kuo et al. teaches a first switching unit connected between said image processing unit and said buffer memory; and a second switching unit connected between said compression unit and said buffer memory (As the image data is alternately read into and out of the ping-pong buffers (1130), there must be a first switching unit connected between said image processing unit (922) and said buffer memory (1130), and a second switching unit connected between said compression unit (924) and said buffer memory (1130), column 11, lines 36-46.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the buffer memory taught by Anderson comprise ping-pong buffers and associated switching units as taught by Kuo et al. as a way of applying a known technique (i.e. ping-pong buffering as taught by Kuo et al.) to a known device (i.e. the image processing apparatus of Anderson) ready for improvement to yield predictable results such as increased processing efficiency due to the parallel processing ping-pong buffering technique.

Consider claim 14, and as applied to claim 13 above, Anderson further teaches that double buffering is performed (column 13, lines 54-57), and that the MCU buffer (204) holds two MCU's (column 14, lines 10-14). Anderson also teaches that alternate embodiments of the MCU input buffers are contemplated to be within the scope of the present invention (column 14, lines 4-7).

However, Anderson does not explicitly teach that said buffer memory comprises first and second buffer memories connected in parallel.

However, in addition to the teachings of Anderson, Kuo et al. teaches that the buffer memory (1130) includes first and second buffer memories (ping-pong buffers, A and B) connected in parallel for data storage, of alternately writing said image data to said first and second buffer memories, and of alternately reading from said first and second buffer memories by said compression unit ("After processing by DSP 922, the data are forwarded to ping-pong buffers A and B 1130 and from there to JPEG hardware 924. DSP 922 and JPEG hardware 924 can be run in parallel (at the same time). Thus, one of the ping-pong buffers (e.g., buffer A) is filled and the data therein are then fed to JPEG hardware 924. JPEG hardware 924 operates on these data while the other ping-pong buffer (e.g., buffer B) is filled. When JPEG hardware 924 is finished with the data from buffer A, it begins to operate on the data in buffer B, and in the meantime buffer A is refilled." column 11, lines 36-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the buffer memory taught by Anderson comprise ping-pong buffers as taught by Kuo et al. as a way of applying a known technique (i.e. ping-pong buffering as taught by Kuo et al.) to a known device (i.e. the image processing apparatus of Anderson) ready for improvement to yield predictable results such as increased processing efficiency due to the parallel processing ping-pong buffering technique.

Consider claim 25, and as applied to claim 1 above, Anderson further teaches that double buffering is performed (column 13, lines 54-57), and that the MCU buffer (204) holds two MCU's (column 14, lines 10-14). Anderson also teaches that alternate embodiments of the MCU input buffers are contemplated to be within the scope of the present invention (column 14, lines 4-7).

However, Anderson does not explicitly teach said buffer memory comprises two line buffers each having a length not less than a length of image data processed by said image processing unit at a single time.

Kuo et al. similarly teaches an image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising an image processing unit (DSP, 922, figure 11) connected to a buffer memory (Ping-Pong Buffers A and B, 1130), which is in turn connected to a compression unit (JPEG hardware, 924).

However, in addition to the teachings of Anderson, Kuo et al. teaches said buffer memory comprises two line buffers each having a length not less than a length of image data processed by said image processing unit a single time (The image processing unit processes lines of image data, column 11, lines 7-54. Column 10, lines 36-40 detail that that the JPEG processing accepts lines of data as its input. Column 11, lines 36-39 detail that the ping-pong buffers are used such that the DSP (922) and JPEG hardware (924) can be run in parallel. Thus each ping-pong buffer (A and B) must have a length not less than a line of image data.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the buffer memory taught by Anderson comprise ping-pong buffers as taught by Kuo et al. as a way of applying a known technique (i.e. ping-pong buffering as taught by Kuo et al.) to a known device (i.e. the image processing apparatus of Anderson) ready for improvement to yield predictable results such as increased processing efficiency due to the parallel processing ping-pong buffering technique.

Consider claim 15, Anderson teaches:

An image processing apparatus (digital camera, figure 1) for performing image processing on captured data of an image of a desired subject (The camera contains a digital signal processor (106) which performs image processing, column 4, lines 24-30, figures 1 and 2B.), comprising:

an image processing part (DSP, 106, figures 1 and 2B); and

a storage unit (memory, 109) provided outside said image processing part (106) and connected to said image processing part (106) by a bus (The storage unit (109) is connected to said image processing part (106) by a bus (113), figure 2B, column 5, lines 56-61.),

said image processing part (106) including:

a buffer memory (MCU buffer, 204) for data storage (The MCU buffer (204) is used to store displayable image data prior to inputting it to JPEG block (205), column 5, lines 17-19.);

an image processing unit (image processing data path, 202) for performing a predetermined process on said captured data to obtain image data ("takes the raw CCD data and converts it into a real image data capable of being displayed", column 5, lines 4-16), and writing said image data to said buffer memory (See figure 2B. The image processing unit (202) outputs the image data to the buffer memory (204).); and

a compression unit (JPEG block, 205) for compressing said image data read from said buffer memory (204) and outputting compressed image data to said storage unit ("A buffer 204 is used to coordinate the transfer of displayable image data to the JPEG block 205, which compresses the data. The compressed displayable image data is then stored in file buffer 213." column 5, lines 17-20, see figure 2B),

wherein an input of said buffer memory (204) is connected, separate from said bus (113), only to said image processing unit (202) to receive only said image data from said image processing unit (See figure 2B. The upper-left input of the buffer memory (204) is connected, separate from said bus (113), only to said image processing unit (202).), and

an output said buffer memory (204) is connected, separate from said bus (113), only to said compression unit (205) to output said image data only to said compression unit (See figure 2B. The lower-right output of the buffer memory (204) is connected, separate from the bus (113), only to said compression unit (205).),

wherein said compression unit (205) is connected to said bus (113, see figure 2B) and outputs said compressed image data directly to said storage unit via said bus ("A buffer 204 is used to coordinate the transfer of displayable image data to the JPEG

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block 205, which compresses the data. The compressed displayable image data is then stored in file buffer 213.” column 5, lines 17-20, see figure 2B. The bus (113) connects the image processing part (106) to the storage unit (109), figure 2B, column 5, lines 56-61.).

Anderson further teaches that double buffering is performed (column 13, lines 54-57), and that the MCU buffer (204) holds two MCU's (column 14, lines 10-14). Anderson also teaches that alternate embodiments of the MCU input buffers are contemplated to be within the scope of the present invention (column 14, lines 4-7).

However, Anderson does not explicitly teach that the buffer memory includes first and second buffer memories connected in parallel for data storage, of alternately writing said image data to said first and second buffer memories, or of alternately reading from said first and second buffer memories by said compression unit.

Kuo et al. similarly teaches an image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising an image processing unit (DSP, 922, figure 11) connected to a buffer memory (Ping-Pong Buffers A and B, 1130), which is in turn connected to a compression unit (JPEG hardware, 924).

However, in addition to the teachings of Anderson, Kuo et al. teaches that the buffer memory (1130) includes first and second buffer memories (ping-pong buffers, A and B) connected in parallel for data storage, of alternately writing said image data to said first and second buffer memories, and of alternately reading from said first and second buffer memories by said compression unit (“After processing by DSP 922, the

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data are forwarded to ping-pong buffers A and B 1130 and from there to JPEG hardware 924. DSP 922 and JPEG hardware 924 can be run in parallel (at the same time). Thus, one of the ping-pong buffers (e.g., buffer A) is filled and the data therein are then fed to JPEG hardware 924. JPEG hardware 924 operates on these data while the other ping-pong buffer (e.g., buffer B) is filled. When JPEG hardware 924 is finished with the data from buffer A, it begins to operate on the data in buffer B, and in the meantime buffer A is refilled.” column 11, lines 36-46).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the buffer memory taught by Anderson comprise ping-pong buffers as taught by Kuo et al. as a way of applying a known technique (i.e. ping-pong buffering as taught by Kuo et al.) to a known device (i.e. the image processing apparatus of Anderson) ready for improvement to yield predictable results such as increased processing efficiency due to the parallel processing ping-pong buffering technique.

Consider claim 16, and as applied to claim 15 above, Anderson does not explicitly teach first and second buffer memories.

Kuo et al. further teaches a first switching unit connected between said image processing unit and said first and second buffer memories; and a second switching unit connected between said compression unit and said first and second buffer memories (As the image data is alternately read into and out of the ping-pong buffers (1130), there must be a first switching unit connected between said image processing unit (922) and

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said first and second buffer memories (1130), and a second switching unit connected between said compression unit (924) and said first and second buffer memories (1130), column 11, lines 36-46.).

Consider claim 20, and as applied to claim 15 above, Anderson further teaches said image processing part (106) connected to store data in and retrieve data from said storage unit (The image processing part (106) is connected to the storage unit (109) via the bus (113), column 5, lines 56-61.).

Consider claim 21, and as applied to claim 15 above, Anderson further teaches:

said image processing part (106) comprises:

a first processing unit (capture data path, 201) for performing a first processing on said captured data and for storing first processed data in said storage unit ("Some of its function include controlling the CCD driver, performing slight compression, collecting statistics regarding the raw CCD data, generating timing references, and loading the input buffer 210 with the slightly compressed raw data." column 4, line 63 through column 5, line 2, figure 2B.); and

a second processing unit (image processing data path, 202) for performing a second processing on said first processed data obtained from said storage unit and outputting said image data to said buffer memory ("takes the raw CCD data and converts it into a real image data capable of being displayed", column 5, lines 4-16.

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See figure 2B. The image processing unit (202) outputs the image data to the buffer memory (204).).

Consider claim 27, Anderson teaches:

An image processing apparatus (digital camera, figure 1) for performing image processing on captured data of an image of a desired subject (The camera contains a digital signal processor (106) which performs image processing, column 4, lines 24-30, figures 1 and 2B.), comprising:

an image processing part (DSP, 106, figures 1 and 2B); and

a storage unit (memory, 109) provided outside said image processing part (106) and connected to said image processing part (106) by a bus (The storage unit (109) is connected to said image processing part (106) by a bus (113), figure 2B, column 5, lines 56-61.),

said image processing part (106) including:

an image processing unit (image processing data path, 202) for performing a predetermined process on said captured data to obtain image data ("takes the raw CCD data and converts it into a real image data capable of being displayed", column 5, lines 4-16), and writing said image data to said buffer memory (See figure 2B. The image processing unit (202) outputs the image data to the buffer memory (204).);

a line memory integrated into said image processing unit (The image processing unit (202) performs "line averaging", and thus must have a line memory, column 5, lines 11-15.);

a compression unit (JPEG block, 205) for compressing said image data (“A buffer 204 is used to coordinate the transfer of displayable image data to the JPEG block 205, which compresses the data. The compressed displayable image data is then stored in file buffer 213.” column 5, lines 17-20, see figure 2B); and

a buffer memory (MCU buffer, 204) connected between said image processing unit (202) and said compression unit (205, see figure 2B); and

wherein an input of said buffer memory (204) is connected, separate from said bus (113), only to said image processing unit (202) to receive only said image data from said image processing unit (See figure 2B. The upper-left input of the buffer memory (204) is connected, separate from said bus (113), only to said image processing unit (202).), and

an output said buffer memory (204) is connected, separate from said bus (113), only to said compression unit (205) to output said image data only to said compression unit (See figure 2B. The lower-right output of the buffer memory (204) is connected, separate from the bus (113), only to said compression unit (205).),

wherein said compression unit (205) is connected to said bus (113, see figure 2B) and outputs said compressed image data directly to said storage unit via said bus (“A buffer 204 is used to coordinate the transfer of displayable image data to the JPEG block 205, which compresses the data. The compressed displayable image data is then stored in file buffer 213.” column 5, lines 17-20, see figure 2B. The bus (113) connects the image processing part (106) to the storage unit (109), figure 2B, column 5, lines 56-61.).

Anderson teaches controlling transfer of compressed image data between the compression unit (205) and the storage unit (109, column 5, lines 17-20). However, Anderson does not explicitly teach a DMA controller controlling the transfer of the compressed image data between the compression unit and the storage unit.

Kuo et al. similarly teaches an image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising an image processing unit (DSP, 922, figure 11) connected to a buffer memory (Ping-Pong Buffers A and B, 1130), which is in turn connected to a compression unit (JPEG hardware, 924).

However, Kuo et al. additionally teaches a DMA controller controlling the transfer of the compressed image data between the compression unit and a storage unit (Kuo et al. teaches that the JPEG hardware (i.e. the compression unit) can be replaced with an image processing hardware system (1230, figure 13) with extended functionality, column 11, line 63 through column 12, line 9. The hardware architecture is DMA based, column 12, lines 10-24. A DMA engine (1430, i.e. DMA controller) is set up for executing the image processing and output to the line writer (650) and the storage unit, column 12, lines 59-67. Figure 14 shows that the DMA controller (1430) outputs data to the line writer (650) and thus the storage unit.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to include a DMA controller as taught by Kuo et al. for controlling the transfer of the compressed image data between the compression unit and the storage unit taught by Anderson as a way of combining prior art elements (i.e.

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the image processing apparatus taught by Anderson and DMA controller taught by Kuo et al.) according to known methods (as taught by Kuo et al.) to yield predictable results such as facilitating the transfer of image data from the compression unit to the storage unit.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 6,563,535) in view of Kuo et al. (US 6,400,471) and Eglit (US 6,002,446).

Consider claim 26, and as applied 1 above, Anderson further teaches that said image processing unit (202) comprises a line memory for storing said captured data (As the image processing unit performs line averaging, it must comprise a line memory, column 5, lines 7-15.). Anderson also teaches that double buffering is performed (column 13, lines 54-57), and that the MCU buffer (204) holds two MCU's (column 14, lines 10-14). Anderson also teaches that alternate embodiments of the MCU input buffers are contemplated to be within the scope of the present invention (column 14, lines 4-7).

However, Anderson does not explicitly teach said buffer memory comprises two line buffers each having a length not less than a length of image data processed by said image processing unit at a single time.

Kuo et al. similarly teaches an image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising an image processing unit (DSP, 922, figure 11)

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connected to a buffer memory (Ping-Pong Buffers A and B, 1130), which is in turn connected to a compression unit (JPEG hardware, 924).

However, in addition to the teachings of Anderson, Kuo et al. teaches said buffer memory comprises two line buffers each having a length not less than a length of image data processed by said image processing unit a single time (The image processing unit processes lines of image data, column 11, lines 7-54. Column 10, lines 36-40 detail that that the JPEG processing accepts lines of data as its input. Column 11, lines 36-39 detail that the ping-pong buffers are used such that the DSP (922) and JPEG hardware (924) can be run in parallel. Thus each ping-pong buffer (A and B) must have a length not less than a line of image data.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have the buffer memory taught by Anderson comprise ping-pong buffers as taught by Kuo et al. as a way of applying a known technique (i.e. ping-pong buffering as taught by Kuo et al.) to a known device (i.e. the image processing apparatus of Anderson) ready for improvement to yield predictable results such as increased processing efficiency due to the parallel processing ping-pong buffering technique.

However, the combination of Anderson and Kuo et al. does not explicitly teach that each line buffer has a length not more than a length of said line memory.

Eglit similarly teaches an image processing apparatus (figure 4, column 11, lines 27-42) with ping pong buffers (420, column 12, lines 14-18).

However, in addition to the teachings of Anderson and Kuo et al., Eglit teaches that each line buffer has a length not more than a length of said line memory (Eglit teaches that the line buffer (420) comprises "two lines" arranged and viewed as two banks. Thus each buffer has a length of one line.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have each line buffer taught by the combination of Anderson and Kuo et al. have a length not more than a length of said line memory as taught by Eglit for the benefit of saving on memory requirements.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALBERT H. CUTLER whose telephone number is (571)270-1460. The examiner can normally be reached on Mon-Thu (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Albert H Cutler/  
Examiner, Art Unit 2622